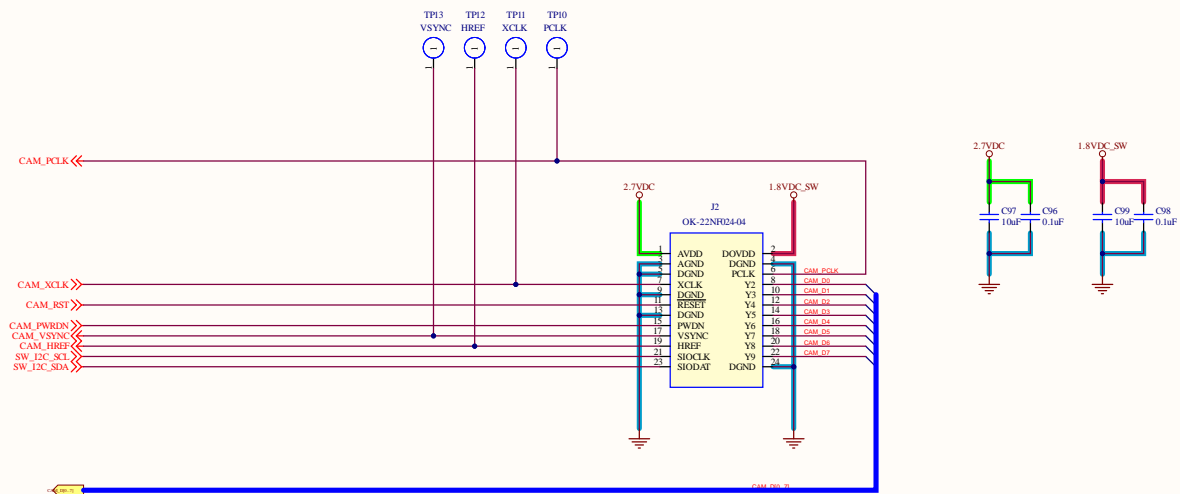
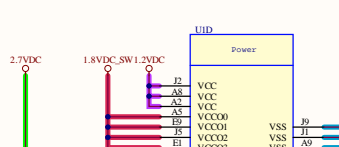
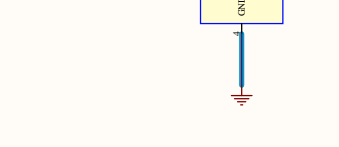
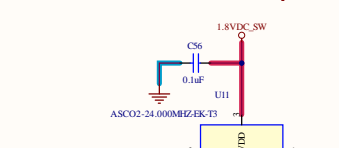
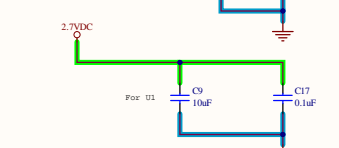
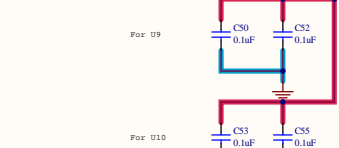
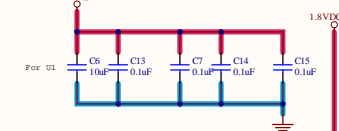
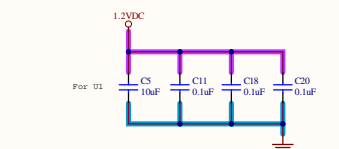
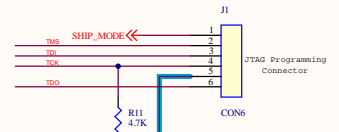
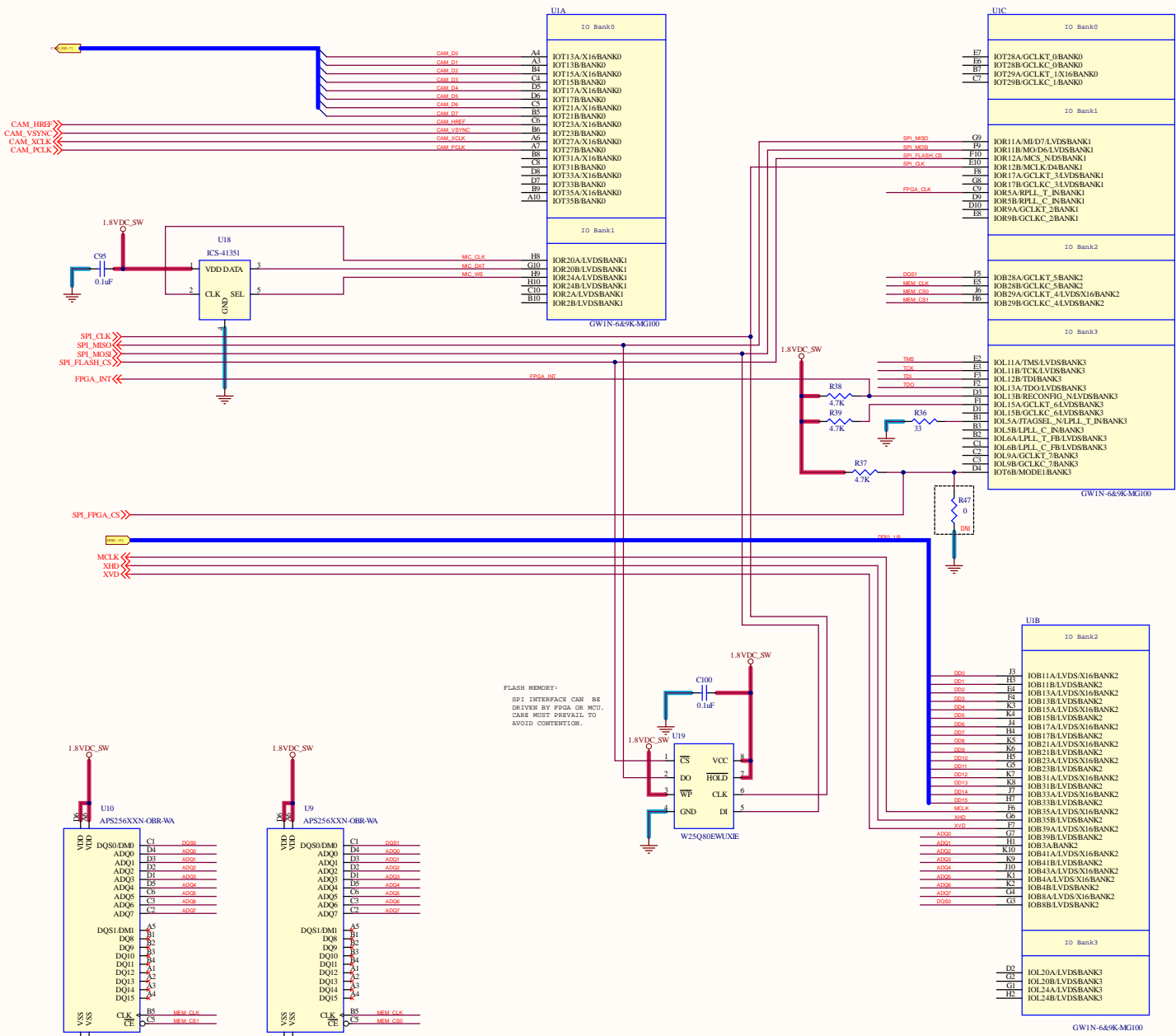


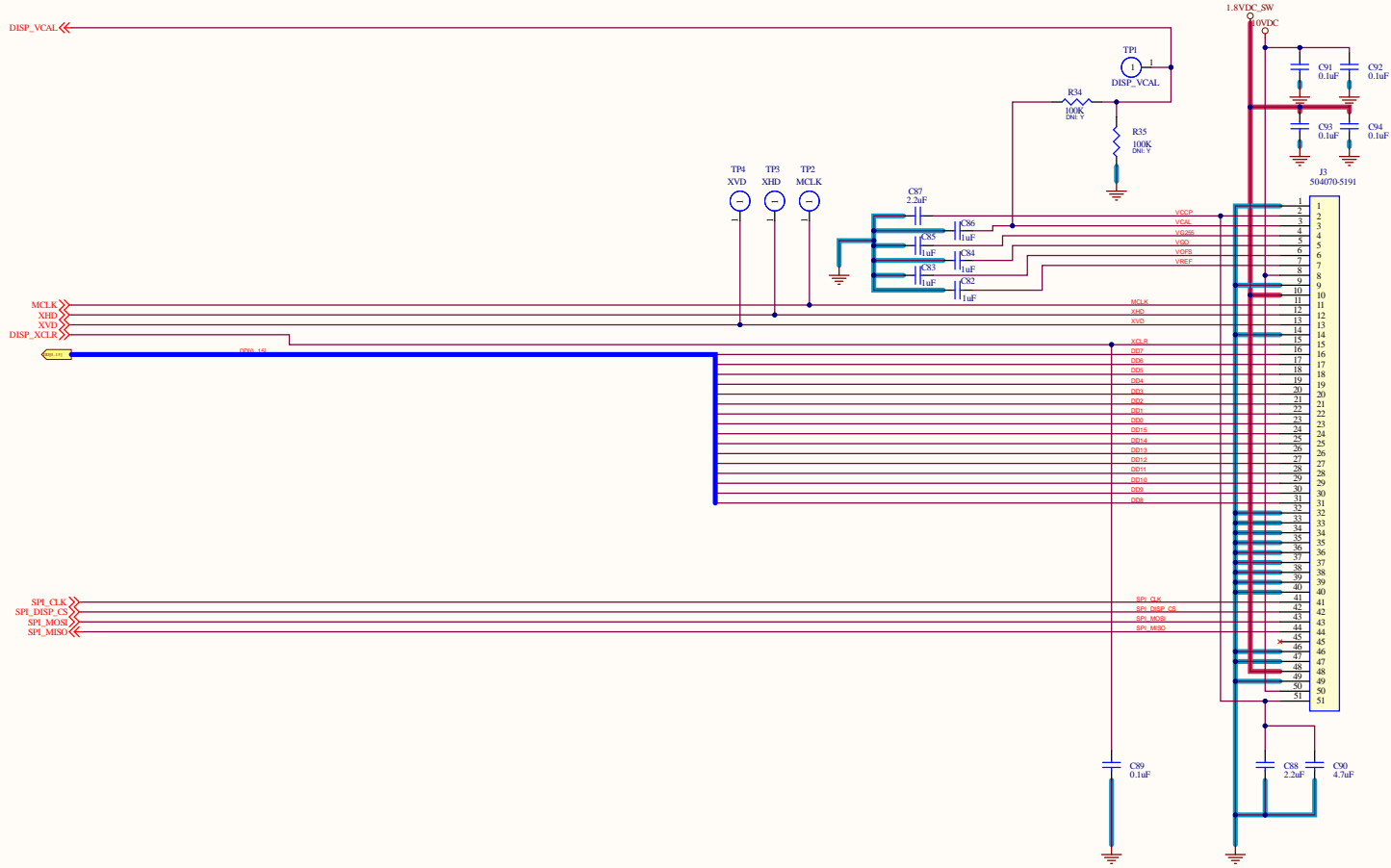
Schematic, MK12 v2		
Rev	Power	Brilliant Labs Ltd.
Size	Document Number	
A	Schematic licensed under: CERN-OHL-P Rev 2	Rev A
Date	Jan 3, 2025	Sheet 1 of 5





FLASH MEMORY:
 SPI INTERFACE CAN BE
 DRIVEN BY FPGA OR MCU.
 DARK MUST PREVAIL TO
 AVOID CONTENTION.

Memory is in x8 mode



MCLK
XHD
XVD
DISP_XCLR

SPI_CLK
SPI_DISP_CS
SPI_MOSI
SPI_MISO

Schematic, MK12 v2		
Rev	OLED Display	Brilliant Labs Ltd.
Size	Document Number	Rev
A	Schematic licensed under: CERN-OHL-P Rev 2	A
Date	Jan 3, 2023	Sheet 5 of 5